Amendments to the Specification:

Please replace paragraph on page 2 beginning at line 9 with the following amended paragraph:

In one embodiment, the system memory coupled to a memory data bus. The memory data bus is coupled to the system bus through a synchronizer. The system memory is adapted to store therein write data words provided on the memory data bus, or have read data words previously stored therein read therefrom and provided on the memory data bus. The read data words and the write data words being provided on the memory bus at a rate twice a predetermined system clock rate. The synchronizer enables the read data words and such write data words to be provided on the system bus in a sequence at the system clock rate. The system includes a trace buffer having a dual port random access memory. The dual port random access memory has a pair of data ports. The dual port random access memory is adapted to store two of the read and write data words from the system data bus fed concurrently to the pair of data ports at two different locations in the dual port random access memory for storage therein at the predetermined system clock rate. The trace buffer control system couples read data words from the system data bus to one of the pair of ports and couples write ~~read~~ data words on the system data bus to the other one of the pair of ports, such read data words and such write data words being retrievable from the dual port random access memory in the same sequence as such read data words and write data words were provided on the system data bus and memory data bus.